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PRELIMINARY INFORMATION

MK74CB163
1 to 16 PECL to CMOS Buffalo™ Clock Driver

Description

The MK74CB163 Buffalo™ is a monolithic CMOS high speed clock driver. It consists of a PECL input to sixteen low-skew output, non-inverting clock drivers. This monolithic solution eliminates any concern for part-to-part skew matching. The MK74CB163 is packaged in the tiny 28 pin SSOP, which uses the same board space as the narrow 16 pin SOIC.

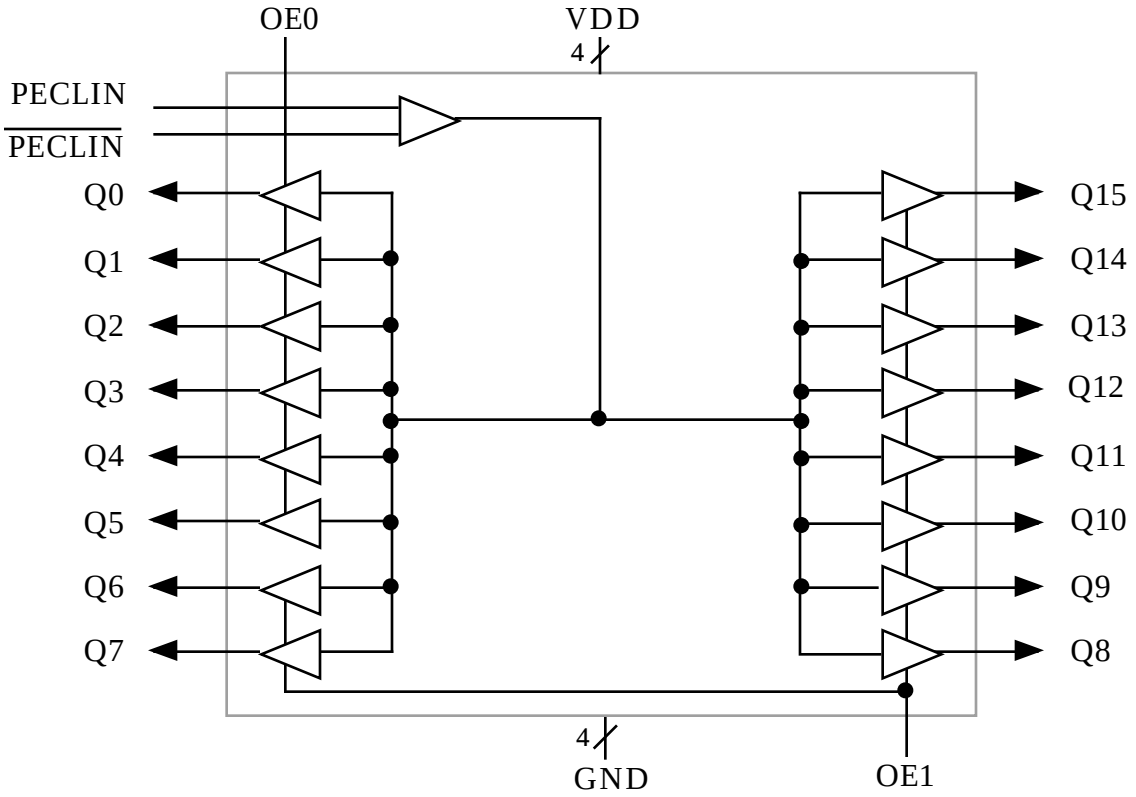
Features

- Tiny 28 pin SSOP (150 mil) package
- One input to sixteen output clock drivers
- Outputs are skew matched to within 250ps
- 3.3 V±10% supply voltage
- Clock speeds up to 156 MHz
- 2 Output Enables allow configuration as 1 to 6, 1 to 10, or 1 to 16 buffers.
- Converts PECL input to CMOS level outputs

Family of ICS Parts

The MK74CB163 Buffalo™ is designed to be used with ICS's clock synthesizer devices. The inputs of the Buffalo are matched to the outputs of ICS clock synthesizers. Consult ICS for applications support.

Block Diagram



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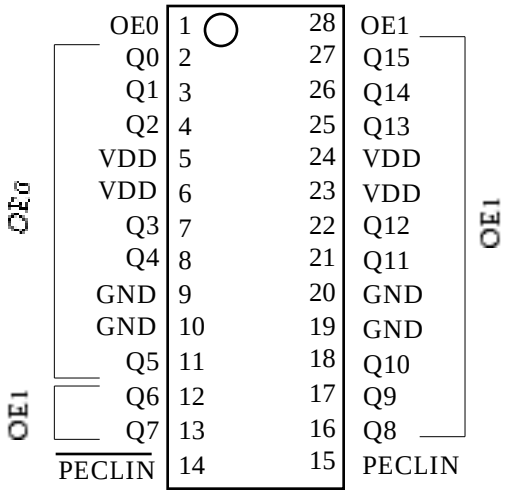
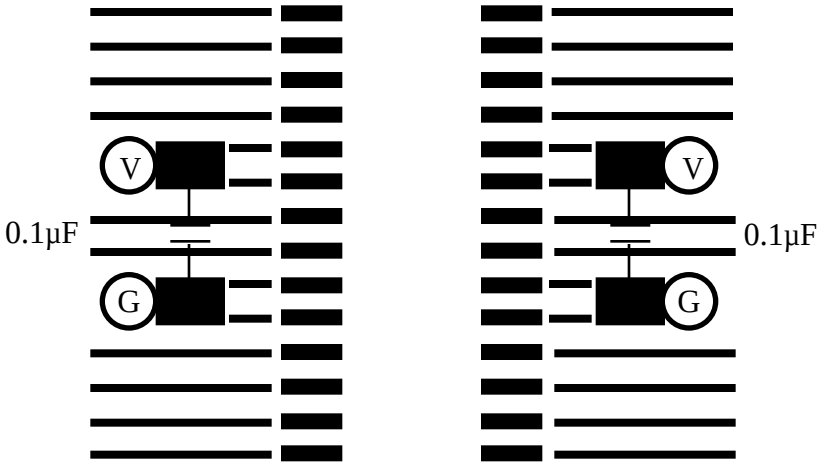
Pin Assignment



Suggested Layout



For simplicity, 33 Ω series termination resistors are not shown for the outputs, but should be placed as close to the device as possible. It is most critical to have the 0.1µF decoupling capacitors closest.

(V) = connect to VDD (G) = connect to GND

Pin Descriptions

Number	Name	Type	Description
1	OE0	I	Output Enable. Tri-states Q0 to Q5 clock outputs when this input is low. Internal pull-up.
2, 3, 4	Q0, Q1, Q2	O	Clock outputs.
5, 6	VDD	P	Power supply. Connect to +3.3V.
7, 8	Q3, Q4	O	Clock outputs.
9, 10	GND	P	Connect to ground.
11, 12, 13	Q5, Q6, Q7	O	Clock outputs.
14	$\overline{\text{PECLIN}}$	I	Complementary PECL input.
15	PECLIN	I	True PECL input.
16, 17, 18	Q8, Q9, Q10	O	Clock outputs.
19, 20	GND	P	Connect to ground.
21, 22	Q11, Q12	O	Clock outputs.
23, 24	VDD	P	Power supply. Connect to +3.3V.
25, 26, 27	Q13, Q14, Q15	O	Clock outputs.
28	OE1	I	Output Enable. Tri-states Q6 to Q15 clock outputs when this input is low. Internal pull-up.

Type: I = Input, O = output, P = power supply connection

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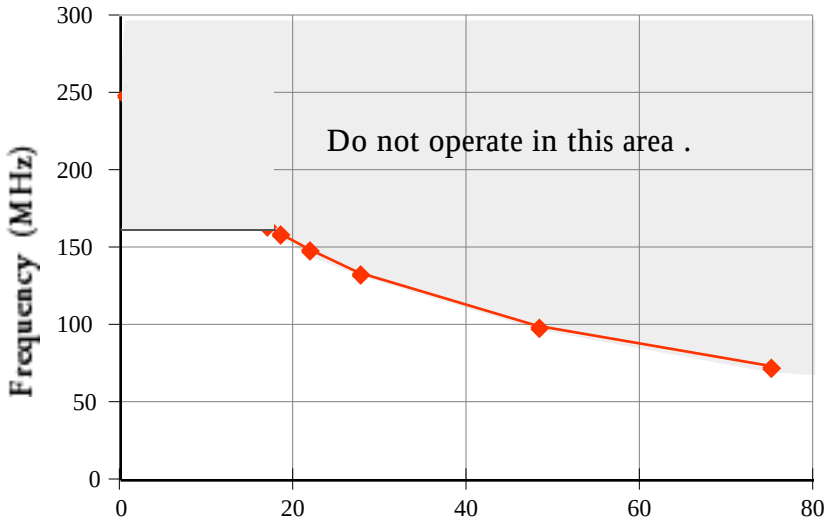
Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (Note 1)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	0.5		VDD+0.5	V
Clock Outputs	Referenced to GND	0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 20 seconds			260	°C
Storage Temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3 V unless noted)					
Operating Voltage, VDD		3.0		3.6	V
Input High Voltage, VIH (OE0, OE1 pins)		2.0			V
Input Low Voltage, VIL (OE0, OE1 pins)				0.8	V
Output High Voltage, VOH	IOH=-12mA	VDD-0.5			V
Output Low Voltage, VOL	IOL=12mA			0.5	V
Operating Supply Current, IDD, at 66.6MHz	No Load		TBD		mA
Short Circuit Current	Each output		±70		mA
On-Chip Pull-up Resistor	OE0, OE1		250		kΩ
Input Capacitance (OE0, OE1)			7		pF
Peak-to-Peak Input Voltage, VPP	PECL inputs	300		1000	mV
Common Mode Range, VCMR	PECL inputs	VDD-1.4		VDD-0.6	V
AC CHARACTERISTICS (VDD = 3.3 V unless noted)					
Input Clock Frequency		0		156	MHz
Propagation Delay with load=15pF					ns
Output Clock Rise Time	0.8 to 2.0V				ns
Output Clock Fall Time	2.0 to 0.8V				ns
Output Clock Rising Edge Skew	Note 2	-250	0	250	ps
Output Enable Time, OE high to output on			5	20	ns
Output Disable Time, OE low to tri-state			5	20	ns
Output Duty Cycle, Load = 15 pF at VDD/2	0-125 MHz	45	50	55	%
Output Duty Cycle, Load = 15 pF at VDD/2	125-156 MHz	40	50	60	%

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. Between any two outputs, with equal loading, measured at VDD/2. The maximum skew between any 2 pins is 250 ps not 500 ps.

Maximum Speed

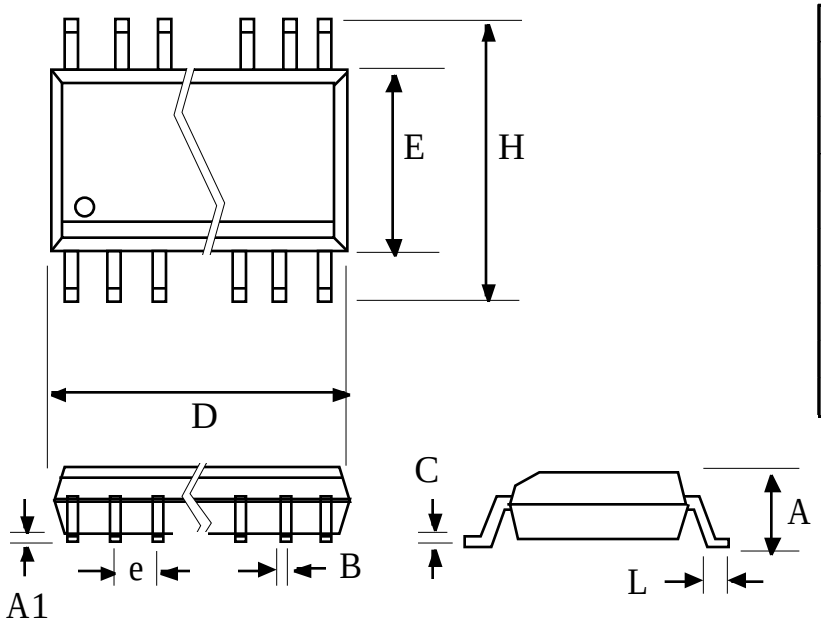
The maximum speed at which the chip can operate can be limited by power dissipation in the package. Graph 1 shows the operating frequency plotted against load capacitance per pin for a die temperature of 125 °C. This is at VDD = 3.3 V, 70 °C and with 33 Ω series termination resistors. The termination resistors are essential because they allow a large proportion of the total power to be dissipated outside the package. Reducing or eliminating the series termination will cause an increase in die temperature. It is not recommended to operate the chip at die temperatures greater than 125 °C. Also note that the load capacitance per pin must include PC board parasitics such as trace capacitance. The MK74CB163 can safely operate up to 156 MHz with all pins loaded at 15 pF.



Graph 1
Maximum Speed

Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC publication no. 95)



28 pin SSOP (QSOP)

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.01	0.10	0.25
B	0.008	0.012	0.20	0.30
C	0.007	0.010	0.19	0.25
D	0.386	0.394	9.80	10.01
E	0.150	0.157	3.81	3.99
H	0.228	0.244	5.79	6.20
e	.025 BSC		0.635 BSC	
L	0.016	0.05	0.41	1.27

Ordering Information

Part/Order Number	Marking	Package	Temperature
MK74CB163R	MK74CB163R	28 pin SSOP (QSOP)	0-70°C
MK74CB163RTR	MK74CB163R	Add Tape & Reel	0-70°C

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